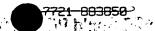
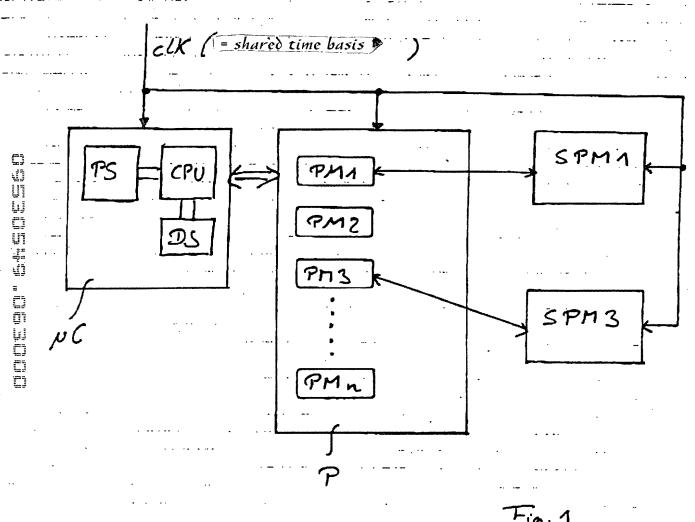


Fig. 1

<i>\oldoy</i>	Sante. Sante.	TOD
8	warte	(25 Marke START START WOVEROOR,
h	warte	MOV A ADC RES
~	festing	_
2	starte wardeny	NOP
7	warte	Mov AGC_RUU,
0	warh	NO P
mulierte	deitakh AGC	CPU





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start of conversion NOP (else if Acts)
now seeme) 14 A> 17 HOV EROOP, Mov ADK RUW, (LS Mark START |wait MOV A ADC RES - Josedspy Gij Wait -- mode for test evaluation + finished conversion DOD 2 start Wait NOP Wait timing clocks? ADC simulated / CPU